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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,839	12/18/2006	Theodor Doll	3222.1430000	8784

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EXAMINER	
SUCH, MATTHEW W	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
09/11/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/570,839	DOLL ET AL.	
	Examiner	Art Unit	
	MATTHEW W. SUCH	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,13 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,13 and 19-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 25 June 2009 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 4, 13 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites "removing both the first photo lacquer and the second metal layer from the surface of the first photo lacquer" in Lines 15-16. However, it is unclear how the first photo lacquer layer can be removed from itself. For the purposes of compact prosecution, the examiner provisionally interprets that the phrase reads "removing both the first photo lacquer and the second metal layer ~~from~~ formed on the surface of the first photo lacquer" in order for the claim to match the Applicant's disclosure. Claims 4, 13 and 26 are indefinite due to their dependency from claim 2.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Eccleston (WO `384).

a. In so far as claim 2 is definite, Eccleston teaches a method for producing, on a substrate, an electronic component with closely adjacent electrodes, the method comprising depositing a first metal layer (Element 4 in Fig. 2; Page 6, Line 21) onto the substrate (Element 2 in Fig. 2; Page 6, Line 19). A first photo lacquer (Element 6 in Figs. 2-3; Page 6, Line 22) is structured onto a surface of the first metal layer, wherein a portion of the surface first metal layer does not have the first photo lacquer thereon (Element 8 in Fig. 3; Page 7, Lines 1-4). The portion of the surface of the first metal layer not having the first photo lacquer is etched (Fig. 4; Page 7, Lines 5-6). The first metal layer is undercut etched so that an overhang (at Element 11 in Fig. 5) is defined by the first photo lacquer (Fig. 4; Page 7, Lines 6-13). A surface of the first photo lacquer and an exposed portion of the substrate where the first metal layer was etched away is exposed to a metal vapor (Page 7, Lines 14-17 describes evaporation of metal over the

entire structure) so that a second metal layer is formed on the surface of the first photo lacquer (since Page 7, Lines 14-17 describes evaporation of metal over the entire structure, and hence on the first photo lacquer) and the exposed portion of the substrate (Element 12 in Fig. 5) where the first metal layer was etched away except in a space between the overhang and the substrate (see Fig. 5 shows no part of Element 12 between the overhang and substrate due to the masking effect of the first photo lacquer). Both the first photo lacquer and the second metal layer are removed from the surface of the first metal layer (Fig. 7; Page 8, Line 6 describes that the first photo lacquer is removed, which also necessarily removes the second metal layer which has been formed across the entire structure, as described on Page 7, Lines 14-17).

b. Regarding claim 26, Eccleston teaches that the structuring comprises structuring the first photo lacquer layer on the surface of the first metal layer so that the first photo lacquer is in direct physical contact with the surface of the first metal layer (see Figs. 2-6; Page 6, Line 22, for example).

6. Claims 2 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by McGehee (Synth. Met., Vol. 85).

c. In so far as claim 2 is definite, McGehee teaches a method for producing, on a substrate, an electronic component with closely adjacent electrodes, the method comprising depositing a first metal layer of Ti/Au (Section 2, Lines 2-4) onto a glass

substrate (Section 2, Line 3). A first photo lacquer of photoresist (Section 2, Line 5) is structured onto a surface of the first metal layer, wherein a portion of the surface first metal layer does not have the first photo lacquer thereon since the photoresist is only covering half of the first metal layer of Ti/Au (Section 2, Lines 4-5). The portion of the surface of the first metal layer not having the first photo lacquer is etched (Section 2, Lines 5-6). The first metal layer is undercut etched so that an overhang is defined by the first photo lacquer (Section 2, Lines 7-8). A surface of the first photo lacquer and an exposed portion of the substrate where the first metal layer was etched away is exposed to a metal vapor so that a second metal layer is formed on the surface of the first photo lacquer and the exposed portion of the substrate where the first metal layer was etched away except in a space between the overhang and the substrate (Section 2, Lines 8-13). Both the first photo lacquer and the second metal layer are removed from the surface of the first metal layer (Section 2, Lines 12-13).

d. Regarding claim 26, McGehee teaches that the structuring comprises structuring the first photo lacquer layer on the surface of the first metal layer so that the first photo lacquer is in direct physical contact with the surface of the first metal layer (Section 2, Lines 4-5).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (`155) in view of Mizusaki (WO `640) in view of Scheifers (`915).

e. Regarding claims 19 and 20, Haung teaches a bottom-gate organic transistor comprising a polymer film substrate (Element 12, Fig. 13; Para. 0023) with a first electrode source (Element 14, Fig. 13) formed on the substrate and a second electrode drain (Element 16, Fig. 13) formed on the substrate. The separation distance between the first and second electrodes is 1 micron or less (Para. 0035). A third electrode gate (Element 22, 34, Fig. 13) is formed in a hole (Element 24, Fig. 13) in the substrate in the separation between the first and second electrodes. An insulating layer (Element 30, Fig. 13) is formed on the third electrode gate. An organic semiconductor layer (Element 28, Fig. 13) is formed on the first electrode, second electrode, and insulator.

Huang does not teach a sealing layer formed on the organic semiconductor. Scheifers teaches a conventional bottom-gate transistor with a sealing layer (Element 16) on the organic semiconductor (Element 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the sealing layer configuration taught by Scheifers in the device of Huang. One would have been motivated to do so since Scheifers teaches that the sealing layer protects the organic

semiconductor from moisture and oxygen, thereby improving the device performance (see Abstract, at least).

While Huang teaches the separation distance between the first and second electrodes is 1 micron or less (Para. 0035), there is no explicit disclosure of about 10 nanometers. However, Mizusaki teaches an organic transistor with the channel length being on the nanometer scale such as 1-20 nm (Page 51, Lines 5-8 and 12-13), and as such the distance between the first and second electrodes being 1-20 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channel length and hence distance between the first and second electrodes to be about 10 nm. One would have been motivated to do so since Mizusaki teaches that a transistor having such dimensions in the nanometer range, including 10 nm, provides greatly improved characteristics compared to conventional transistors. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum value involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See MPEP § 2144.05.

f. Regarding claim 21 and 22, Huang teaches that the electrodes can be formed of conductive electroplatable materials without explicitly citing the conventional materials of gold and chromium (Para. 0025).

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either gold or chromium, since such materials provide low contact resistance and are conventional electroplatable materials and Scheifers discloses

using gold for a gate, source and drain (see Para. 0025). It has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). See MPEP § 2144.07.

g. Regarding claim 27, the language of the claim is directed towards the process of making the electronic component of claim 19. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. As such, the language claim 27 only requires the structure of the electronic device of claim 19, which does not distinguish the invention from Huang in view of Mizusaki in view of Scheifers, who teaches the

structure as claimed. The claim does not add any additional structural features to the final device that are not already set forth by claim 19.

9. Claims 23-25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (`155) in view of Mizusaki (WO `640) in view of Scheifers (`915) in view of Higuchi (J. Poly. Sci., Part B: Poly. Phys., Vol. 34; provided as evidence and supplied with Office Action dated 28 April 2009).

h. Haung teaches a bottom-gate organic transistor comprising a polycarbonate substrate (Element 12, Fig. 13; Para. 0023, Line 5) with a first electrode source (Element 14, Fig. 13) formed on the substrate and a second electrode drain (Element 16, Fig. 13) formed on the substrate. Higuchi teaches that polycarbonate is a glass (see Higuishi who states that polycarbonate is a polymer glass), which is a glass that is different than SiO_2 (see Higuchi "PC glasses"). The separation distance between the first and second electrodes is 1 micron or less (Para. 0035). A third electrode gate (Element 22, 34, Fig. 13) is formed in a hole (Element 24, Fig. 13) in the substrate in the separation between the first and second electrodes. An insulating layer (Element 30, Fig. 13) is formed on the third electrode gate. An organic semiconductor layer (Element 28, Fig. 13) is formed on the first electrode, second electrode, and insulator.

Huang does not teach a sealing layer formed on the organic semiconductor. Scheifers teaches a conventional bottom-gate transistor with a sealing layer (Element 16) on the organic semiconductor (Element 14). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to use the sealing layer configuration taught by Scheifers in the device of Huang. One would have been motivated to do so since Scheifers teaches that the sealing layer protects the organic semiconductor from moisture and oxygen, thereby improving the device performance (see Abstract, at least).

While Huang teaches the separation distance between the first and second electrodes is 1 micron or less (Para. 0035), there is no explicit disclosure of about 10 nanometers. However, Mizusaki teaches an organic transistor with the channel length being on the nanometer scale such as 1-20 nm (Page 51, Lines 5-8 and 12-13), and as such the distance between the first and second electrodes being 1-20 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channel length and hence distance between the first and second electrodes to be about 10 nm. One would have been motivated to do so since Mizusaki teaches that a transistor having such dimensions in the nanometer range, including 10 nm, provides greatly improved characteristics compared to conventional transistors. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum value involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See MPEP § 2144.05.

i. Regarding claims 24 and 25, Huang teaches that the electrodes can be formed of conductive electroplatable materials without explicitly citing the conventional materials of gold and chromium (Para. 0025).

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either gold or chromium, since such materials provide low contact resistance and are conventional electroplatable materials and Scheifers discloses using gold for a gate, source and drain (see Para. 0025). It has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). MPEP § 2144.07.

j. Regarding claim 28, the language of the claim is directed towards the process of making the electronic component of claim 19. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. As such, the language claim 27 only

requires the structure of the electronic device of claim 19, which does not distinguish the invention from Huang in view of Mizusaki in view of Scheifers, who teaches the structure as claimed. The claim does not add any additional structural features to the final device that are not already set forth by claim 19.

Allowable Subject Matter

10. In so far as definite, claims 4 and 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

A search of the prior art does not disclose or reasonably suggest a method for producing, on a substrate, an electronic component with closely adjacent electrodes, the method comprising: depositing a first metal layer onto the substrate; structuring a first photo lacquer on a surface of the first metal layer, wherein a portion of the surface of the first metal layer does not have the first photo lacquer thereon; etching the portion of the surface of the first metal layer not having the first photo lacquer; undercut etching the first metal layer so that an overhang is defined by the first photo lacquer; exposing, to a metal vapor, a surface of the first photo lacquer and an exposed portion of the substrate where the first metal layer was etched away so that a second metal layer is formed on the surface of the first photo lacquer and the exposed portion of the substrate where the first metal layer was etched away except in a space between the overhang and the substrate; and removing both the first photo lacquer and the second metal layer formed

on the surface of the first photo lacquer; etching a hole into the substrate at a position other than a position of the first metal layer and the second metal layer; depositing a third metal layer onto the substrate, the first metal layer, and the second metal layer; applying an insulator onto the third metal layer; applying an organic semiconductor onto the third metal layer and the insulator; and applying a sealing layer onto the organic semiconductor.

Response to Arguments

12. Applicant's arguments with respect to claims 2, 4, 13 and 19-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Scheinert (Appl. Phys. Lett., Vol. 84) teaches a method of forming electrodes on a substrate by undercut etching a metal layer using a photo lacquer mask.

Contact Information

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW W. SUCH whose telephone number is (571)272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Rose can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew W. Such/
Examiner, Art Unit 2891